TSMC-02-1264

October 15, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

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Subject: Serial No. 10/618,793 07/15/03

Kuo-Chi Tu

METHOD OF IMPROVING THE TOP PLATE ELECTRODE STRESS INDUCTING VOIDS FOR 1T-RAM PROCESS

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 20, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/20/03

U.S. Patent 6,136,688 to Lin et al., "High Stress Oxide to Eliminate BPSG/SiN Cracking," discloses a high compressive stress oxide layer to eliminate cracks in a subsequently deposited tensile stress layer such as SiON.

U.S. Patent 6,414,376 to Thakur et al., "Method and Apparatus for Reducing Isolation Stress in Integrated Circuits," discloses a silicon-rich SiN layer that relieves stress in a SiN layer.

U.S. Patent 5,883,001 to Jin et al., "Integrated Circuit Passivation Process and Structure," discloses a PE-SiON or SiN layer having compressive stress with an overlying PSG layer having tensile stress as a stress buffer.

U.S. Patent 5,503,882 to Dawson, "Method for Planarizing an Integrated Circuit Topography," describes a PECVD oxide layer under a TEOS oxide layer where the compressive stress of the PECVD oxide layer offsets the TEOS layer's tensile stress.

U.S. Patent 6,221,794 to Pangrie et al., "Method of Reducing Incidence of Stress-Induced Voiding in Semiconductor Interconnect Lines," teaches annealing before interlayer dielectric deposition to avoid stress-induced voids.

U.S. Patent 5,583,077 to Wang et al., "Integrated Dual Layer Passivation Process to Suppress Stress-Induced Metal Voids," discloses that compressive stress appears in a PSG layer if the layer is exposed to humidity for a time before a SiN layer is deposited over it.

U.S. Patent 6,468,855 to Leung et al., "Reduced Topography DRAM Cell Fabricated Using a Modified Logic Process and Method for Operating Same," describes stress avoidance by performing high thermal cycles prior to P+/N+ shallow junction formation and salicidation.

U.S. Patent 6,287,962 to Lin, "Method for Making a Novel Graded Silicon Nitride/Silicon Oxide (SNO) Hard Mask for Improved Deep Sub-Micrometer Semiconductor Processing," describes a graded SNO layer where the top of the layer provides an ARC function.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-1264	10/618,793
Applicant: Kuo-Chi Tu	
Filing Date: 07/15/03	Group Art Unit:

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	6136688	10/24/00	Lin et al.	438	624	10/20/99
	6414376	7/2/02	Thakur et al.	257	640	2/19/99
	5883001	3/16/99	Jin et al.	438	624	11/7/94
	5503882	4/2/96	Dawson	427	579	4/18/94
	6221794	4/24/01	Pangrle et al.	438	792	12/8/98
	5583077	12/10/96	Wang et al.	437	240	4/4/95
	6468855	10/22/02	Leung et al.	438	239	1/29/01
	6287962	9/11/01	Lin	438	638	11/30/00

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant